Hi3518C Economical HD IP Camera SoC

Brief Data Sheet

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Hi3518C Economical HD IP Camera SoC

Key Specifications

Processor

- ARM926
  - Up to 400 MHz
  - 16 KB I-cache, 16 KB D-cache

Video Encoding

- H.264 baseline profile
- H.264 main profile Level4.0
- MJPEG/JPEG baseline

Video Encoding Performance

- At most 2-megapixel resolution for H.264 encoding
- Real-time H.264&JPEG encoding of multiple types of streams: 720p@30 fps+ QVGA@30 fps+720p@1 fps JPEG snapshot
- JPEG snapshot of 720P@30 fps
- CBR, VBR, and ABR, ranging from 16 kbit/s to 20 Mbit/s
- Encoding frame rate, ranging from 1/16 frame/s to 30 frame/s
- Eight ROIs
- OSD overlay of eight regions before encoding

Intelligent Video Analysis

- Integrated intelligent analysis acceleration engine, supporting motion detection, boundary guard, and video diagnosis

Video and Graphic Processing

- 3D denoise, pre-processing, image enhancement, edge enhancement, and de-interlace
- Anti-flicker processing for output videos and graphics
- 1/16x to 8x video scaling
- 1/2x to 2x image scaling
- OSD overlay pre-processing for eight areas during encoding
- Hardware graphics overlay post-processing for the videos at two layers (video layer and graphics layer 1)

ISP

- Adjustable AWB and AE function
- Highlight compensation, backlight compensation, gamma correction, and color enhancement
- Defect pixel correction, denoise, and digital image stabilizer
- Defogging
- Lens distortion correction
- Mirror and flip
- Digital WDR and tone mapping
- PC and ISP tuning tools

Audio Codec

- Voice codec in compliance with multiple protocols by using software
- G.711, ADPCM, and G.726 encoding
- Echo cancellation

Security Engine

- AES, DES, and 3DES encryption and decryption algorithms by using hardware
- Digital watermark

Video Interfaces

- Input
  - 8-/10-/12-bit RGB Bayer input, a maximum of 74.25 MHz clock frequency
  - BT.601
  - BT.656
  - Compatibility with mainstream CMOSs provided by SONY, Aptina, OmniVision, and Panasonic
  - Compatibility with the CCD sensor
  - Various sensor voltages
  - Programmable sensor clock output
  - At most 2-megapixel input resolution
- Output
  - One 1080p@30 fps BT.1120 VO interface for connecting to the external HDMI or SDI interface

Audio Interfaces

- Integrated audio codecx1, 16-bit voice inputs and outputs

Peripheral Interfaces

- POR
- High-accurate RTC
- A dual-channel SAR-ADC
- UARTx2
- I^2Cx1, and GPIOs
- SDIO 2.0x1, SDHC
- USB 2.0 hostx1
- RMII and MII modes, 10 Mbit/s or 100 Mbit/s full-duplex or half-duplex mode, providing PHY clock output

External Memory Interfaces

- DDR2 or DDR3 SDRAM
  - 16-bit DDR2/DDR3@400 MHz
  - Maximum capacity of 1Gbit
- SPI/NOR flash: 1-, 2-, or 4-bit SPI/NOR flash
- NOR flash boot mode

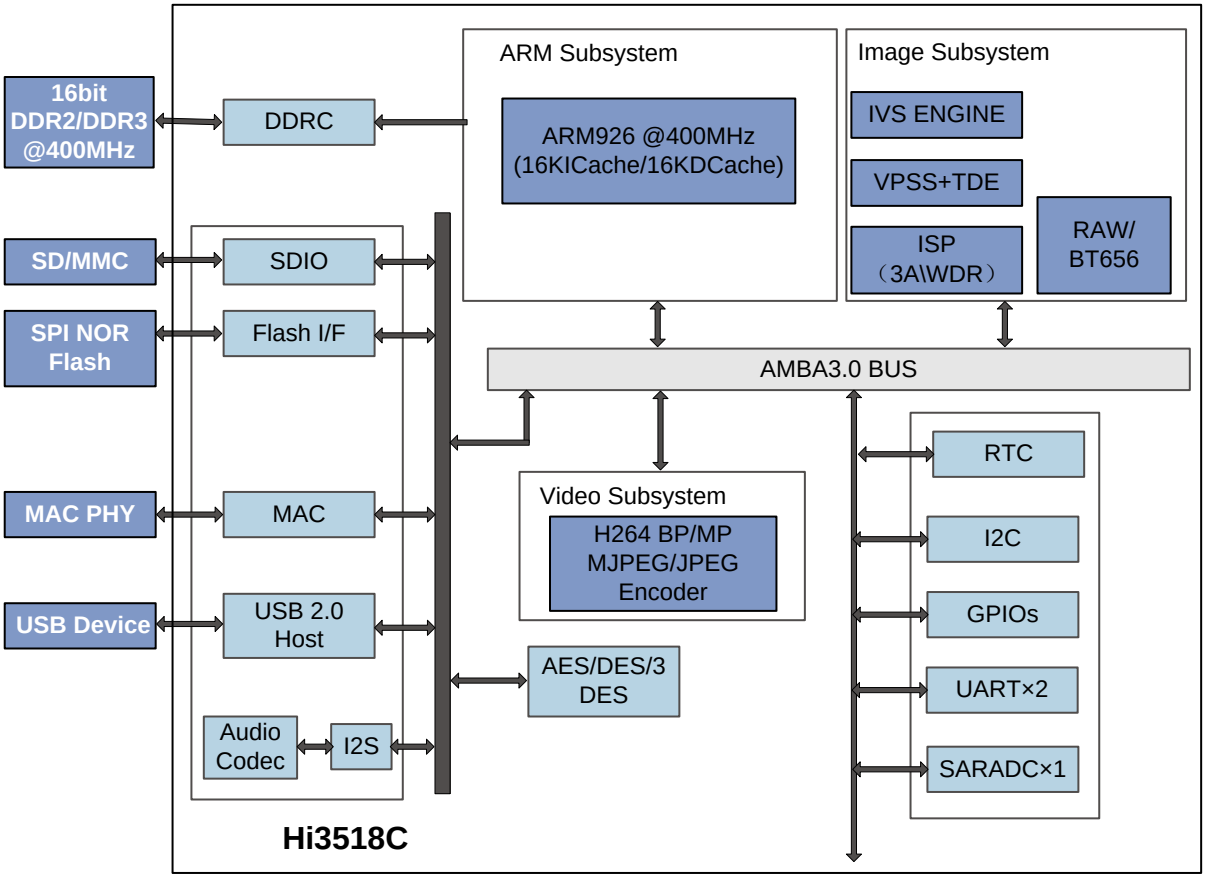
SDK

- SDK based on Linux-3.0.y
- High-performance H.264 PC decoding library

Physical Specifications

- Power consumption
  - Typical power of 700 mW
  - Multiple-level power-saving modes
- Operating voltage
  - 1.2 V core voltage
  - 3.3 V I/O voltage, and 3.8 V tolerance voltage
  - 1.5 V or 1.8 V DDR SDRAM voltage (1.5 V for DDR3 or 1.8 V for DDR2)
- Package
  - 176-pin QFP RoHS Package, body size 20mm x 20mm with 0.4mm pitch

Functional Block Diagram



Traditional VGA MJPEG cameras cannot meet current surveillance needs because there is a continuous increase in network bandwidth, widespread usage of mobile applications, and high requirements for high-definition videos. The Hi3518C is an economical SoC designed for high-definition surveillance applications. It has a new-generation ISP and H.264 encoder and uses an optimized pre-encoding image processing algorithm. These features enable the Hi3518C to provide high-quality images at low encoding bit rates. It supports lens distortion correction to meet the requirements in undistorted indoor surveillance applications. It also uses advanced low-power technology and architecture and QFP package, facilitating PCB surface mounting. Because the Hi3518C integrates the POR, RTC, and audio CODEC, and supports various sensor voltages and clock outputs, the EBOM costs for the Hi3518C HD IP camera are significantly reduced. In addition, the Hi3518C SDK supports Linux 3.0 kernel and allows customers to select components flexibly

Hi3518C IPC Solution