Hi3521 H.264 Codec Processor

Brief Data Sheet

Issue 03

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Hi3521 H.264 Codec Processor

Key Specifications

Processor Core

- ARM Cortex A9 @ max. 930 MHz
  - 32 KB L1 I-cache and 32 KB L1 D-cache
  - 256 KB L2 cache

Video Encoding and Decoding Protocols

- H.264 Baseline Profile Level 5.0
- H.264 Main Profile Level 5.0
- MJPEG/JPEG Baseline

Video Encoding and Decoding

- H.264&JPEG encoding and decoding of multiple streams:
  - 16CIF@30 fps+16QCIF@30 fps encoding+16CIF@30 fps decoding+JPEG snapshot D1@8 fps
  - 1x720p@30 fps+VGA@30 fps encoding+7D1@30 fps+ 7CIF@30 fps encoding+1D1@30 fps decoding+JPEG snapshot@4 fps
  - 8x960H@30 fps+8CIF@30 fps encoding+1x960H@30 fps decoding+ JPEG snapshot 960H@4 fps
  - 8D1@30 fps+8CIF@30 fps encoding+4D1@30 fps decoding+JPEG snapshot D1@4 fps
  - 1x720p@30 fps+VGA@30 fps encoding+4D1@30 fps+ 4CIF@30 fps encoding+4D1@30 fps decoding+JPEG snapshot@4 fps
  - 4x960H@30 fps+4CIF@30 fps encoding+4x960H@30 fps decoding+ JPEG snapshot 960H@4 fps
  - 4x720p Real-Time Decoding
- CBR, VBR, or ABR ranging from 16 kbit/s to 40 Mbit/s
- Encoding frame rate ranging from 1 fps to 60 fps
- ROI encoding
- Color-to-gray encoding

Intelligent Video Analysis

- Integrated intelligent analysis acceleration engine, supporting motion detection, boundary security, and video diagnosis

Video and Graphic Processing

- Video pre- and post-processing, including de-interlacing, image enhancement, edge enhancement, and 3D denoising
- Anti-flicker for output videos and graphics
- 1/8x to 8x video scaling
- 1/2x to 2x graphic scaling
- OSD overlay of eight regions before encoding
- Alpha blending of video layers and graphics layers

Audio Encoding and Decoding

- ADPCM, G.711, and G.726 hardware encoding
- Software decoding complying with various protocols

Security Engine

- AES, DES, and 3DES encryption and decryption
- Digital watermark

Video Interfaces

- Video input interfaces
  - 4xBT.656@108/144 MHz for 16CIF/8x960H real-time inputs
  - 2xBT.1120@148.5 MHz for 2x1080p real-time inputs
  - 4xBT.656@148.5 MHz for 4x720p real-time inputs
- Video output interfaces
  - HDMI 1.3+VGA+CVBSx2 outputs. The HDMI and VGA outputs can share the same source
  - 1xLCD, 1xBT1120@148.5 MHz, or 1xBT656@27 MHz digital video output. The LCD and BT.1120 outputs share the same source. The BT.656 and CVBS outputs share the same source
  - Maximum 1080p@60 fps for HDMI or VGA
  - Three graphics layers in RGB1555 or RGB8888 format, with the maximum resolution of 1920x1080
  - One hardware cursor layer in RGB1555 or RGB8888 format, with the maximum resolution of 128x128
  - One independent video PIP layer

Audio Interfaces

- Four I^2S interfaces
  - Two for input
  - One for input or output
  - One for HDMI I^2S output

Ethernet Port

- One GMAC port
  - RGMII or MII mode
  - 10/100 Mbit/s full-duplex or half-duplex mode
  - 1000 Mbit/s full-duplex mode
  - TOE for reducing the CPU usage

Peripheral Interfaces

- Two SATA 2.6 interfaces
  - PM
  - eSATA
- Four UART interfaces
- One SPI, supporting four CSs
- One IR interface, one I^2C interface, and multiple GPIO interfaces
- One SDIO 2.0 interface, supporting a maximum of 32 GB capacity
- Two USB 2.0 host ports, supporting hub

Memory Interfaces

- One 16- or 32-bit DDR2/DDR3 SDRAM controller interface
  - Maximum frequency of 620 MHz
  - ODT
  - Maximum capacity of 1 GB
  - Automatic power consumption control
- SPI NOR flash interfaces
  - 1-, 2-, or 4-bit SPI NOR flash interfaces
  - Two CSs
  - Maximum capacity of 32 MB for each CS
- NAND flash interfaces
  - 8-bit data width
  - SLC or MLC
  - 1-, 4-, or 24-bit ECC

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- Built-in 2 KB BOOTROM and 10 KB SRAM

Boot Modes

- BOOTROM
- SPI NOR flash
- NAND flash

SDK

- Linux 3.0-based SDK
- High-performance H.264 PC decoding library

Physical Specifications

- Power consumption
  - 3.5 W typical power consumption
  - Multi-level power-saving control
- Operating voltage
  - 1.0 V core voltage
  - 3.3 or 2.5 V I/O voltage and 5 V margin voltage
  - 1.5 V or 1.8 V DDR2/DDR3 SDRAM interface voltage
  - Operating temperature ranging from –20°C (–4°F) to +70°C (+158°F)
- Package
  - RoHS, EHS-FCBGA449
  - Ball pitch: 0.8 mm (0.031 in.) in the core power area or 0.65 mm (0.026 in.) in other areas
  - Body size: 19 mm x 19 mm (0.75 in. x 0.75 in.)

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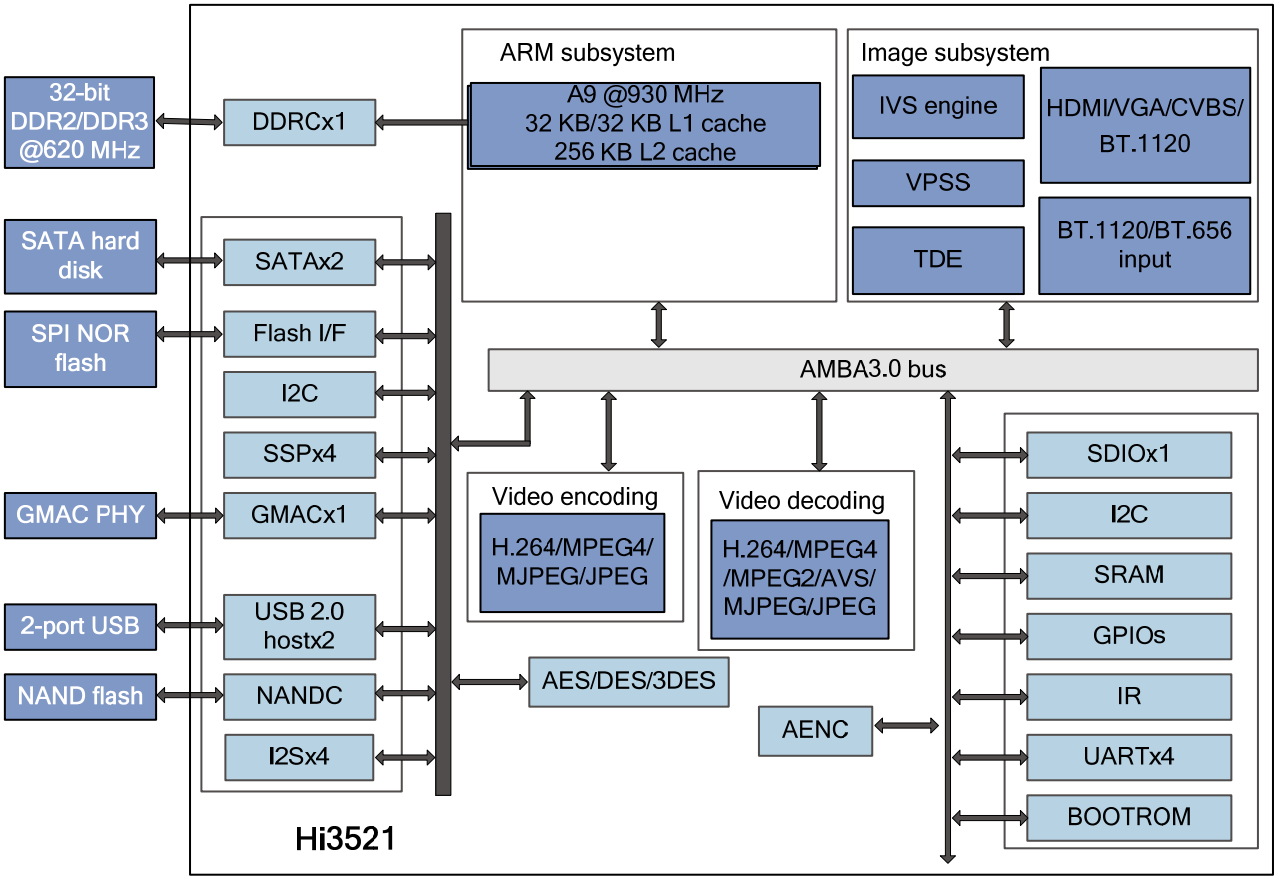
Functional Block Diagram



The Hi3521 is a professional high-end SoC designed for multi-channel D1 and HD DVRs and NVRs. With a high-performance A9 processor, a dedicated TOE, and an engine supporting up to 8-channel D1 real-time encoding and decoding, the Hi3521 meets the rising demand for HD and network applications. The Hi3521 also provides an outstanding video engine, various encoding/decoding algorithms, and multi-channel HD output capability. These features guarantee users a high-quality image experience. In addition, the Hi3521 supports various highly-integrated peripheral interfaces to meet customer requirements for functionality, features, and image quality, while reducing the EBOM cost.

DVRs (Each with a Hi3521)

DVR for 8D1+8CIF Encoding+4D1 Decoding

- 8D1+8CIF dual-stream real-time encoding+16 fps D1 JPEG snapshot+4D1 real-time decoding
- HDMI+VGA 1080p@60 fps outputs from the same source+2-channel CVBS outputs

DVR for 8x960H+8CIF Encoding+1x960H Decoding

- 8x960H+8CIF encoding+16fps 960H JPEG snapshot+1x960H real-time decoding

DVR for 16CIF Encoding+16QCIF Encoding+16CIF Decoding

- 16CIF +16QCIF dual-stream real-time encoding+16CIF real-time decoding
- HDMI+VGA 1080p@60 fps outputs from the same source+2-channel CVBS outputs

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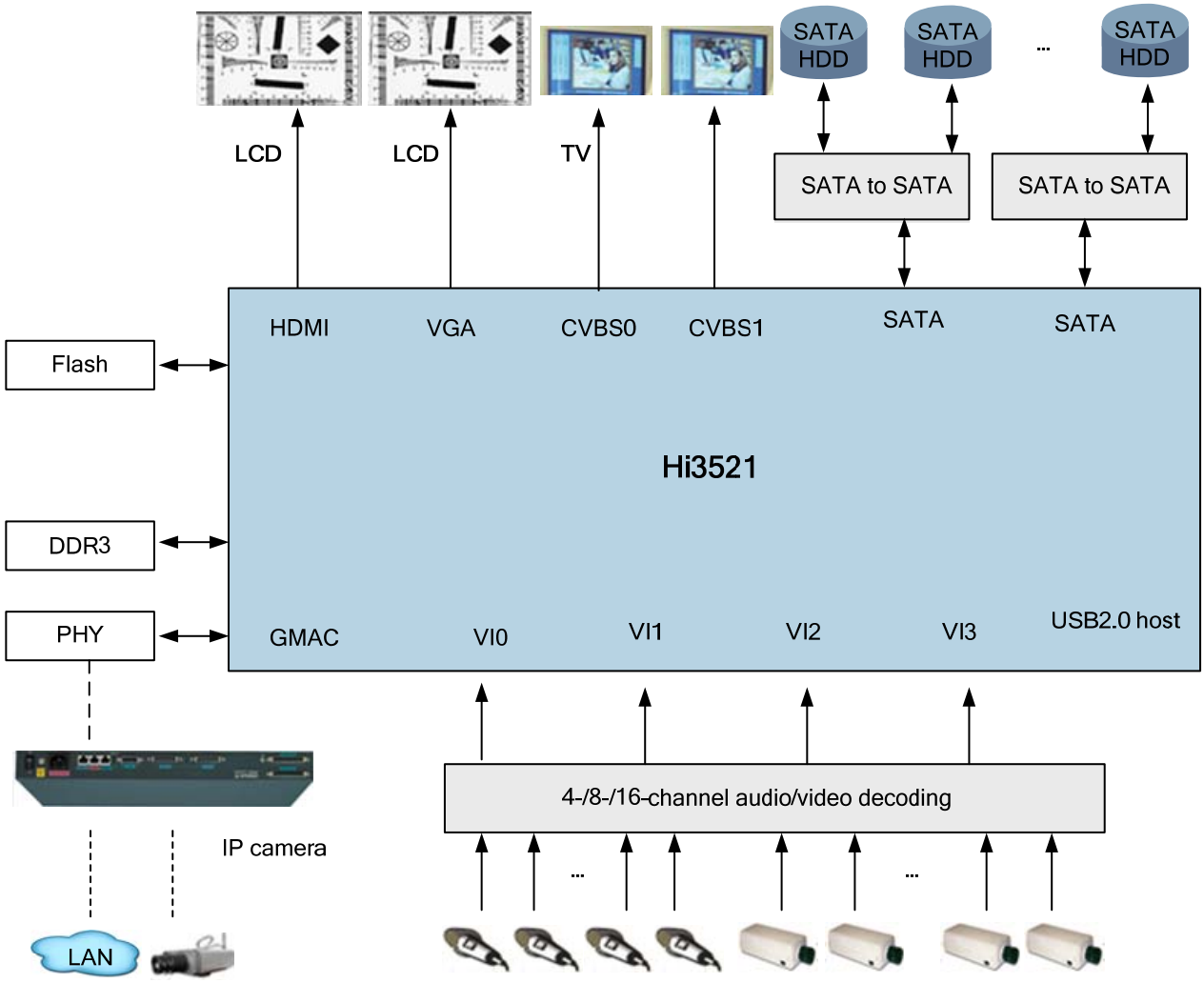

NVR with a Hi3521

4x720p Real-Time Decoding

- 4x720p decoding
- HDMI+VGA 1080p@60 fps outputs from the same source+2-channel CVBS outputs

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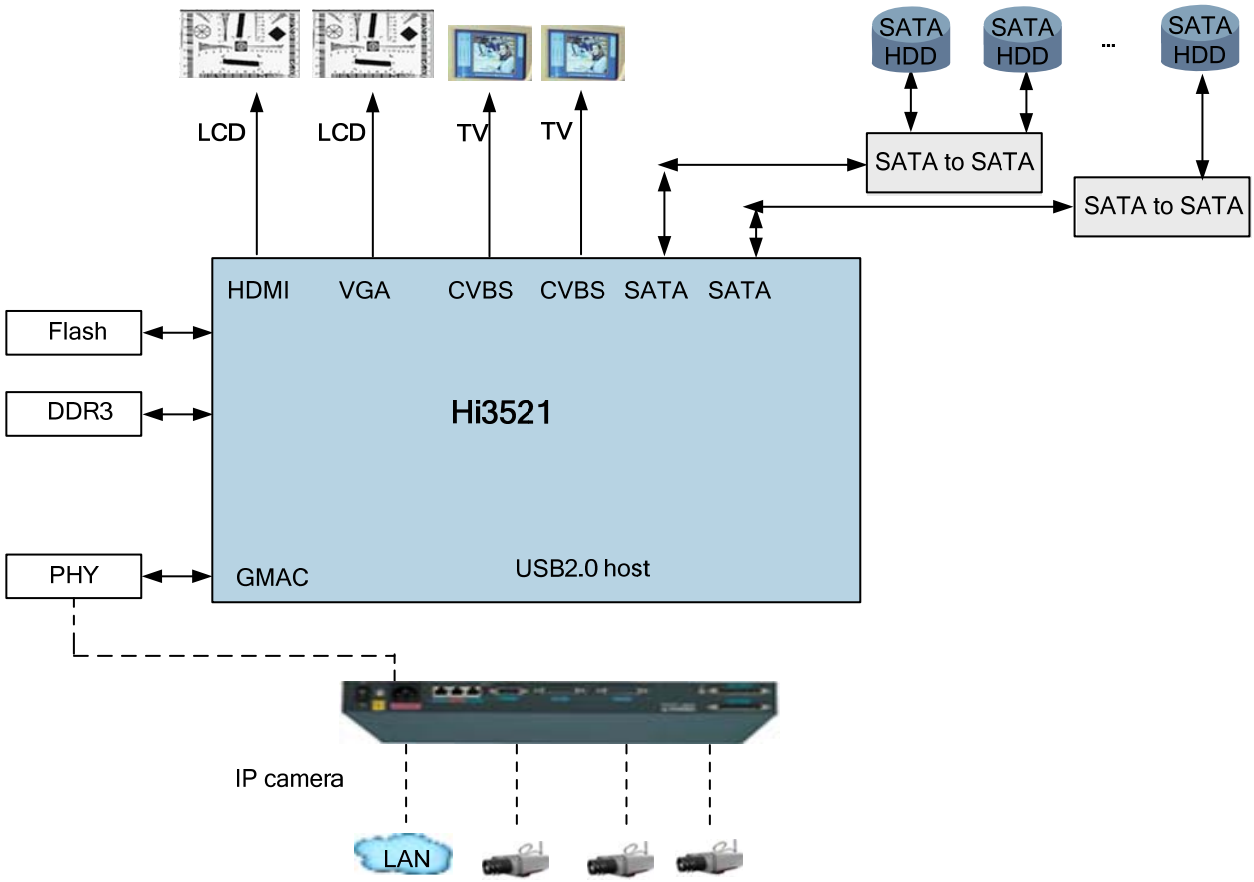

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